2814

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/916,555
Filing Date	July 26, 2001
First Named Inventor	Wang et al.
Group Art Unit	2814
Examiner Name	M.D. Pizarro-Crespo
Attorney Docket Number	2102397-911400

Total Number of Pages in This Submission: 15

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☒ Amendment/Reply with Appendix A
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition to Covert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

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PATENT TRADEMARK OFFICE

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-1896. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

GRAY CARY WARE & FREIDENRICH LLP

Dated: October 22, 2002

By: _____

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CERTIFICATE OF MAILING

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Typed or printed name	Kathleen LaBrie		
Signature	Kathleen LaBrie	Date	October 22, 2002

Atty Dckt Number: 2102397-911400

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Chi Hsin Wang et al.

Application No. 09/916,555

Filed: July 26, 2001

For: A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH LOW RESISTANCE SOURCE REGIONS AND HIGH SOURCE COUPLING (as amended herein)

Group Art Unit: 2814

Examiner: M. D. Pizarro-Crespo

RESPONSE TO OFFICE ACTION MAILED JULY 26, 2002

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GRAY CARY WARE & FREIDENRICH Date: 10/22/02

By: Kathleen LaBrie

Kathleen LaBrie

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed on July 26, 2002 please amend the above identified application as follows:

I. CLEAN VERSION OF AMENDED SPECIFICATION, TITLE AND CLAIMS, AND NEWLY ADDED CLAIMS

A. Please amend the title to read:

--A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH LOW RESISTANCE SOURCE REGIONS AND HIGH SOURCE COUPLING--

B. Please substitute the paragraph on page 12, lines 4-24 with the following paragraph:

--As shown in Fig. 2N, first and second regions 50/80 form the source and drain for each cell (those skilled in the art know that source and drain can be switched during operation). The channel region 92 for each cell is the portion of the substrate that is in-between the source and drain 50/80. Poly blocks 68 constitute the control gate, and poly layer 14 constitutes the floating gate. Oxide layers 32, 36, 46 and 48 together form an insulation layer that is disposed adjacent to and over floating gate 14, to isolate it from conductive block 54 and conductive layer 52. Oxide layers 36 and 64 together form an insulation layer that isolates the conductive block 54 and conductive layer 52 from the control gates 68. The control gates 68 have one side aligned to the edge of the second region 80, and are disposed over part of the channel regions 92. Control gates 68 have lower portions 70 that are disposed adjacent to the floating gates 14 (insulated therefrom by oxide layer 64), and upper protruding portions 72 that are disposed (extend) over a portion of adjacent poly layers 14 (insulated therefrom by oxide layers 64). A notch 94 is formed by the protruding portion 72, where the sharp edge 66 of floating gate 14 extends into the notch 94. Each floating gate 14 is disposed over part of the channel region 92, is partially overlapped at one end by the control gate 68, and partially overlaps the first region 50 with its other end. Conductive blocks 54 and the conductive layers 52/56 together form source lines 96 that extend across the columns of memory cells. Upper portions 62 of source lines 96 extend over but are insulated from the floating gates 14, while lower portions 60 of source lines 96 are adjacent to but insulated from floating gates 14. As illustrated in the Fig. 2N, the process of the present invention forms pairs of memory cells that mirror each other. The pairs of mirrored memory cells are insulated from other cell pairs by oxide layer 76, nitride spacers 78 and BPSG 86.--

C. Please substitute each of the following claims for the corresponding pending claim in this application:

27. (Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed over and insulated from a portion of said channel region and a portion of the first region, wherein the floating gate consists of a first portion and a second portion integrally formed together;

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate first portion and not the floating gate second portion; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to and insulated from the floating gate, and the second control gate portion being disposed over and insulated from the floating gate second portion and not the floating gate first portion.

30. (Amended) The device of claim 27, further comprising:

an insulation layer disposed between the floating gate and the control gate, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

31. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a pair of electrically conductive floating gates each disposed over and insulated from a portion of one of the channel regions and a portion of the first region, wherein each of the floating gates consists of a first portion and a second portion integrally formed together,

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the floating gate first portions and not the floating gate second portions; and

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed adjacent to and insulated from one of the floating gates and the second control gate portion is disposed over and insulated from the second portion and not the first portion of the one floating gate.

35. (Amended) The device of claim 31, wherein each of the memory cell pairs further comprises:

an insulation layer disposed between each of the floating gates and each of the control gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

D. Please add the following new claims:

37. (New) The device of claim 27, further comprising:

insulation material disposed between the source region second portion and the floating gate first portion, and having a thickness for permitting voltage coupling therebetween.

38. (New) The device of claim 31, wherein each of the memory cell pairs further comprises:

insulation material disposed between the source region second portion and each of the floating gate first portions, and having a thickness for permitting voltage coupling therebetween.